S3 Technologies

WE OFFER IEEE PROJECTS FOR MCA FINAL YEAR STUDENT PROJECTS, ENGINEERING PROJECTS AND TRAINING, PHP PROJECTS, JAVA AND J2EE PROJECTS, ASP.NET PROJECTS, NS2 PROJECTS, MATLAB PROJECTS AND IPT TRAINING .

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2019 - 2020 VLSI IEEE PROJECTS

S.NO	Project Code	IEEE 2019 VLSI Project Titles	Domain	Lang/Year
1	S301	A 0.3-V 37-nW 53-dB SNDR Asynchronous Delta–Sigma Modulator in 0.18-µm CMOS	LOW POWER	VLSI/2019
2	S302	A 12-bit, 2.5-bit/Phase Column-Parallel Cyclic ADC	LOW POWER	VLSI/2019
3	S303	A 16-bit 2.0-ps Resolution Two-Step TDC in 0.18-µm CMOS Utilizing Pulse-Shrinking Fine Stage With Built-In Coarse Gain Calibration	LOW POWER	VLSI/2019
4	S304	A Dynamic Timing Error Avoidance Technique Using Prediction Logic in High-Performance Designs	LOW POWER	VLSI/2019
5	S305	A Dynamic Timing Error Avoidance Technique Using Prediction Logic in High-Performance Designs	LOW POWER	VLSI/2019
6	S306	A Wideband Low-Noise Variable-Gain Amplifier with a 3.4 dB NF and up to 45 dB gain tuning range in 130 nm CMOS	LOW POWER	VLSI/2019
7	S307	A Wideband Low-Noise Variable-Gain Amplifier with a 3.4 dB NF and up to 45 dB gain tuning range in 130 nm CMOS	LOW POWER	VLSI/2019
8	S308	Analysis, Comparison, and Experimental Validation of a Class AB Voltage Follower With Enhanced Bandwidth and Slew Rate	LOW POWER	VLSI/2019
9	S309	Column-Selection-Enabled 10T SRAM Utilizing Shared Diff-VDD Write and Dropped-VDD Read for Power Reduction	LOW POWER	VLSI/2019
10	S310	Designing Efficient Circuits Based on Runtime-Reconfigurable Field-Effect Transistors	LOW POWER	VLSI/2019
11	S311	Fully Differential 4-V Output Range 14.5-ENOB Stepwise Ramp Stimulus Generator for On-Chip Static Linearity Test of ADCs	LOW POWER	VLSI/2019
12	S312	Low-Power Near-Threshold 10T SRAM Bit Cells With Enhanced Data-Independent Read Port Leakage for Array Augmentation in 32-nm CMOS	LOW POWER	VLSI/2019
13	S313	Multiloop Control for Fast Transient DC–DC Converter	LOW POWER	VLSI/2019

14	S314	Radiation-Hardened 14T SRAM Bitcell With Speed and Power Optimized for Space Application	LOW POWER	VLSI/2019
15	S315	A 0.9-V 12-Gb/s Two-FIR Tap Direct DFE With Feedback-Signal Common-Mode Control	HIGH SPEED AND SIGNAL PROCESSING	VLSI/2019
16	S316	A 2.4-GHz Frequency-Drift-Compensated Phase-Locked Loop With 2.43 ppm/°C Temperature Coefficient	HIGH SPEED AND SIGNAL PROCESSING	VLSI/2019
17	S317	A High-Flexible Low-Latency Memory-Based FFT Processor for 4G, WLAN, and Future 5G	HIGH SPEED AND SIGNAL PROCESSING	VLSI/2019
18	S318	An Accurate and Noise-Resilient Spread-Spectrum Clock Tracking Aid for Digitally-Controlled Clock and Data Recovery Loops	HIGH SPEED AND SIGNAL PROCESSING	VLSI/2019
19	S319	An Analog LO Harmonic Suppression Technique for SDR Receivers	HIGH SPEED AND SIGNAL PROCESSING	VLSI/2019
20	S320	An Area-Efficient 128-Channel Spike Sorting Processor for Real-Time Neural Recording With 0.175 µW/Channel in 65-nm CMOS	HIGH SPEED AND SIGNAL PROCESSING	VLSI/2019
21	S321	Analysis and Optimization of Multisection Capacitive DACs for Mixed-Signal Processing	HIGH SPEED AND SIGNAL PROCESSING	VLSI/2019
22	S322	CMOS First-Order All-Pass Filter With 2-Hz Pole Frequency	HIGH SPEED AND SIGNAL PROCESSING	VLSI/2019
23	S323	Design of Reconfigurable Digital IF Filter with Low Complexity	HIGH SPEED AND SIGNAL PROCESSING	VLSI/2019
24	S324	Feedforward-Cutset-Free Pipelined Multiply–Accumulate Unit for the Machine Learning Accelerator	HIGH SPEED AND SIGNAL PROCESSING	VLSI/2019
25	S325	Line Coding Techniques for Channel Equalization: Integrated Pulse-Width Modulation and Consecutive Digit Chopping	HIGH SPEED AND SIGNAL PROCESSING	VLSI/2019
26	S326	Multiplier-free Implementation of Galois Field Fourier Transform on a FPGA	HIGH SPEED AND SIGNAL PROCESSING	VLSI/2019
27	S327	Power-Efficient Gm-C DSMs With High Immunity to Aliasing, Clock Jitter, and ISI	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2019
28	S328	A Combined Arithmetic-High-Level Synthesis Solution to Deploy Partial Carry-Save Radix-8 Booth Multipliers in Datapaths	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2019
29	S329	A Decoder for Short BCH Codes With High Decoding Efficiency and Low Power for Emerging Memories	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2019

30	S330	A High-Throughput Hardware Accelerator for Lossless Compression of a DDR4 Command Trace	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2019
31	S331	An Energy-efficient Accelerator based on Hybrid CPU-FPGA Devices for Password Recovery	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2019
32	S332	Area–Delay–Energy Efficient VLSI Architecture for Scalable In-Place Computation of FFT on Real Data	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2019
33	S333	Area-Time Efficient Streaming Architecture for FAST and BRIEF Detector	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2019
34	S334	Chaos-Based Bitwise Dynamical Pseudorandom Number Generator on FPGA	AREA EFFICIENT/TIMING & DELAY REDUCTION	VLSI/2019
35	S335	Efficient Design for Fixed-Width Adder-Tree	AREA EFFICIENT/IMING & DELAY REDUCTION	VLSI/2019
36	S336	Hardware-Efficient Post-processing Architectures for True Random Number Generators	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2019
37	S337	Multistage Linear Feedback Shift Register Counters With Reduced Decoding Logic in 130-nm CMOS for Large-Scale Array Applications	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2019
38	S338	New Majority Gate Based Parallel BCD Adder Designs for Quantum-dot Cellular Automata	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2019
39	S339	Rapid Balise Telegram Decoder with Modified LFSR Architecture for Train Protection Systems	AREA EFFICIENT/ TIMING & DELAY REDUCTION	VLSI/2019